Verification of Error Models Through Low-Level Simulation

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An important issue in fault-injection is the verification of the error models as representative of realistic errors. One technique to perform this verification involves the injection of faults using a low-level circuit simulator. The errors that are eventually propagated to the chip-pin or higher level level can be considered to be those errors which are most likely to occur, based on those faults. These errors should form the basis for the error models used in higher fault level injection mechanisms.

We have used a mixed-mode simulator that can propagate transient faults from the device level to the chip-pin level. Simulations involving an HS1602 avionics microprocessor used in Boeing aircraft showed that a specific error probability for every pin could be found depending upon the location and type of the low-level fault. These error probabilities should be used as the basis for error models of chip-pin errors for this particular chip. If a software-based register modification fault injection mechanism is being used, then the low-level simulation need only propagate the low-level fault to a register that can be injected.

Most word-based error models are simple: single-bit or double-bit flip, or set or zero a word. Error model verification can not only determine which models should be used, but also which bits should be corrupted in the bit-flip models. This can be especially important if the target of the injection is an instruction, the bits of which do not all hold equal significance. Non-word based models can also be considered, such as errors in control signals.

In a sense, this method can be viewed as a composite mix-mode simulation, with the generation of error models being similar to the generation of a fault dictionary. Since most practical fault injection mechanisms are only intended to emulate the effects of low-level faults, the use of verified error models increases the confidence that valid fault-injection is being performed.

In addition to a circuit simulator, other low-level simulators can be used to form error models. For instance, we have developed a wear-out simulation environment that can predict

permanent faults in VLSI circuits. Other simulators can be created to consider other low-level faults, such as memory faults due to radiation and disk faults due to wear-out.

The disadvantage of this method is the need to perform a low-level simulation for each chip to be injected. Also, the selection of the low-level faults and the inputs used to drive that fault are very significant. However, some form of error model verification is necessary, because the results of fault injection experiments based on unverified error models may not be realistic.